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Fundamentals Plasmonic Logic Gates at Nano Scale Structure and 1550 nm Wavelength

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Abstract

This article posits, simulates, designs, and implements all-optical logic gates that use nano-rings Insulator-Metal-Insulator (IMI) plasmonic waveguides (NOT, OR, AND). The suggested plasmonic gates' structure has been designed and numerically simulated by two dimensions (2-D) structure using the Finite Element Method (FEM). The proposed device's performance is evaluated using four criteria: transmission, modulation depth, extension ratio, and insertion loss. The proposed structure was built with silver and glass materials. The suggested plasmonic gates' functionality was achieved by using the concepts of destructive and constructive interferences. Numerical simulations show that at 1550 nm operating wavelength, the suggested plasmonic gates could be implemented in a single structure with a transmission threshold of (0.5). This device had the following characteristics: transmission exceeding 100% in one state of NOT and exceeding 200% in one state of OR and AND gates, medium and high Extension Ratio values, so small footprint, and very high MD values. Future access to nanophotonic integrated circuits will be made possible by this technology, which is also thought to be a crucial component of all-optical computers.

Introduction

The discovery of the Wood's anomaly, a midportion of the light spectrum that a metal grating emits, in early 1902 sparked the beginning of scientific study on Plasmonics [1]. Later, a physical explanation

for the Lord Rayleigh phenomena [2], which describes an anomaly in the spectrum of the light that is diffracted within a wavelength in which an unintentionally dispersed wave arises on surface, was put forward. Afterward, the semi-stationary polarized waves resonating over the surface of the metal were anticipated. This energy loss is caused by cohesion, when excited electrons in the metal, which were afterward named surface plasmons [3]. Surface plasmon polaritons (SPPs) are electromagnetic waves confined on metal-dielectric interfaces and associated with the propagation of free electronic oscillations on the metal surface. [4-6], and are thought to have the greatest potential for creating nanophotonic devices [7-9]. Researchers have gotten interested in optical devices based on (SPPs) in new times, as the need of high-bandwidth, high-speed data transmission has grown. SPPs devices outdo electrical device restrictions such as the delay in the rate at which data are sent and significant heat generation. (SPPs) aid in overcoming the limit of diffraction in classic optical systems and sub-wavelength processing of light. This trait motivated researchers to focus on micro guiding structure that restrict sub-wavelength light. Plasmonic waveguides show great potential in terms of steering patterns of sub-wavelength light, since (SPPs) is the interplay of electromagnetic waves and free electrons of metals propagating across metalinsulating or insulating-metal interfaces [10,11]. Several Plasmonic waveguiding structures have been proposed like resonators [12], modulators [13], switches [14], nanocavities [15], nanowires [16], Bragg reflectors [15], multi/demultiplexers [17], and logic gates [18-21]. In the logic gates' field, each structure has a distinct means of realizing the function, various geometries, different materials, different numbers and kinds of logic gates, different resonance wavelength values, and different transmission values. This paper proposes a structure that can execute three plasmonic logic gates (NOT, OR, AND) simultaneously. Materials, structure parameters, resonance wavelength, and transmission threshold are all same. A Nano-rings resonator and Insulator-Metal-Insulator (IMI) plasmonic Nano-waveguides are accustomed to build the structure. COMSOL Multiphysics (version 5.4) simulation results that have been relied upon are based on the Finite Element Method (FEM). In the future, this technique will make nanophotonic integrated circuits accessible, and it has been thought of as a fundamental component for all-optical computers. This scientific article is structured as follows: Section 2 goes over all of the methodology's procedures, resources, and mathematical models. Sections 3 present and discuss the results. Section 4 compares this work to prior ones. Section 5 concludes with closing comments.

Theoretical concepts

The SPPs signal is guided between dielectric-metal interfaces via plasmonic waveguides. Recently, two types of waveguides have been widely employed in plasmonic structures: insulator-metal-insulator

(IMI) and metal-insulator-metal (MIM) plasmonic waveguides. IMI waveguides have a longer propagation length, reduced propagation loss, and are simpler to fabricate [18]. Because of these advantages, we chose IMI plasmonic waveguides over MIM plasmonic waveguides. As illustrated in Fig. 1, the suggested framework for performing Plasmonic gates (NOT, OR, AND) comprises of two nano-ring resonators and three stripes. The stripes and the nano-ring resonator are made of metal, namely silver, whereas the rest of the framework is made of dielectric, namely glass.

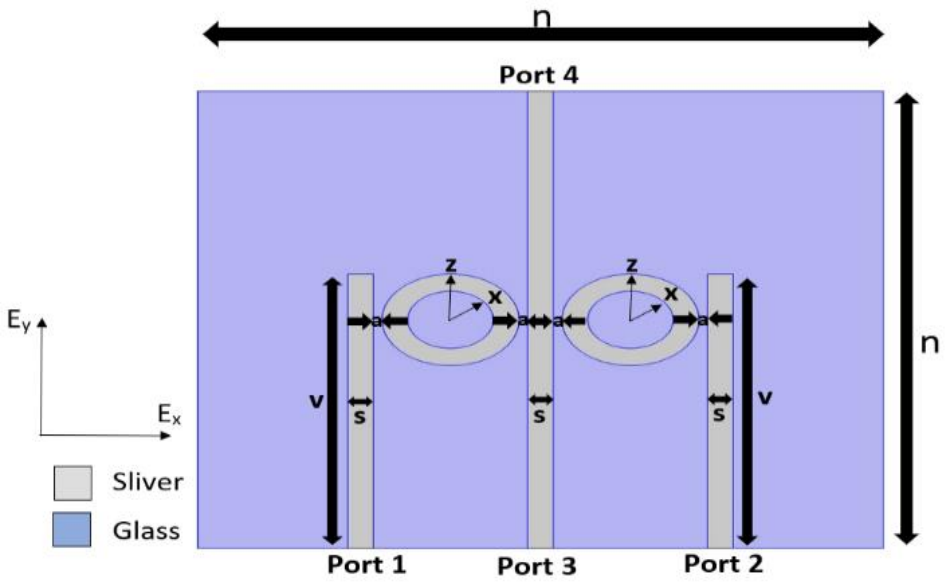


Figure. 1 Framework of plasmonic gates

Silver permittivity is based on Johnson and Christy data [22], and the dielectric refractive index is 1.52 for the Glass [20]. Table 1 shows characteristics of the suggested framework.

Table 1. Structure parameters of the proposed design

Parameter	Description	Value (nm)
n	Width and Length of the structure	400
v	Length of the side stipe	240
s	Stripes width	15
a	Distance between stripes and nano-rings	5
x	The smaller radius of nano-ring	25
z	The bigger radius of nano-ring	40

The dimensions, size, and materials used in plasmonic logic gate structures are all the same. Because it is the ideal wavelength for optical telecommunication systems, the operational wavelength of 1550 nm was chosen. The resonance wavelength 1550 nm is made achievable by the proposed structure's size, shape, materials, and structural factors. Maxwell equations were solved using the two-dimensional (2D) structure in COMSOL Multiphysics program (version 5.4) using the FEM method. A plane wave having Transverse Magnetic (TM) components Ex, Ey, and Hz is exposed to the framework, which has four ports as illustrated in Fig. 1. At 1550 nm, the suggested all-optical logic gates are functional based on four criteria: transmission [19], contrast ratio (CR) [19], modulation depth (MD) [19], and insertion loss (IL) [23]. Table 2 shows the performance's equations.

Table 2. Performance's equations

symbol	Equation
T	$\frac{Output\ optical\ Power}{Input\ Optical\ Power}$
CR (dB)	$10 \log \left(\frac{P_{out}\|ON/min}{P_{out}\|OFF/max}\right)$
MD (%)	$\left(\frac{T_{ON}\|Max - T_{OFF}\|Min}{T_{ON}\|Max}\right) \times 100\%$
IL (dB)	$-10 \log \left(\frac{P_{out}\|ON/min}{P_{in}}\right)$

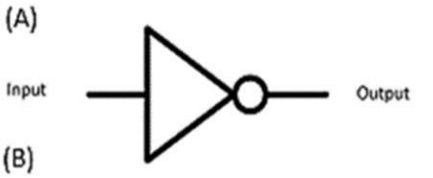
Pout represents output optical power, where Pin represents optical power of the input, which is 1 uW, which reached a single input port or control port. The primary idea for achieving the function of the suggested all-optical logic gates is to use constructive and destructive interferences. Constructive interference is caused by two or more signals with the same phase. Contrarily, destructive interference is brought on by the difference in phase between the incident light signals on the structure. Each gate's truth table in logic 1 and logic 0 is implemented using this idea.

Results

In both OFF and ON states, the transmission is determined, and a transmission threshold value is chosen to determine whether the state is off or on. A series of specifications led to the selection of the transmission threshold value of 0.5 in this design to implement the three logic gates [24].

NOT Logic gate

As illustrated in Fig. 1, the present suggested structure implements a NOT gate by designating executors 1 and 2 as control executors, executors 3 and 4 as input and output, respectively. It is a kind of logic gate that reverses the input signal and is also referred to as an inverter. The symbol circuit and truth table are depicted in Fig. 2(a) and (b), respectively.



(B)

Input	Output
0	1
1	0

Figure. 2 (A) Symbol of NOT gate (B) Fact table of NOT gate

To function as a NOT gate, it is possible to employ subversive interference between control and input signals. When the control executors are ON and its phase is 0° and the input executor is OFF, the output executor is ON and its transmission greater than the defined threshold. When the light is launched to the input port with a phase 0° and control ports with a phase 180°, 45° respectively the output executor's status can be regarded as OFF With an extremely low transmission level, and this is a result for destructive interference. Fig. 3 depicts the transmission versus wavelength range curve for the plasmonic NOT gate. Fig. 4 (a) and (b) depicts the distribution of magnetic field of both cases. Table 3 describes the validation of suggested plasmonic NOT gate.

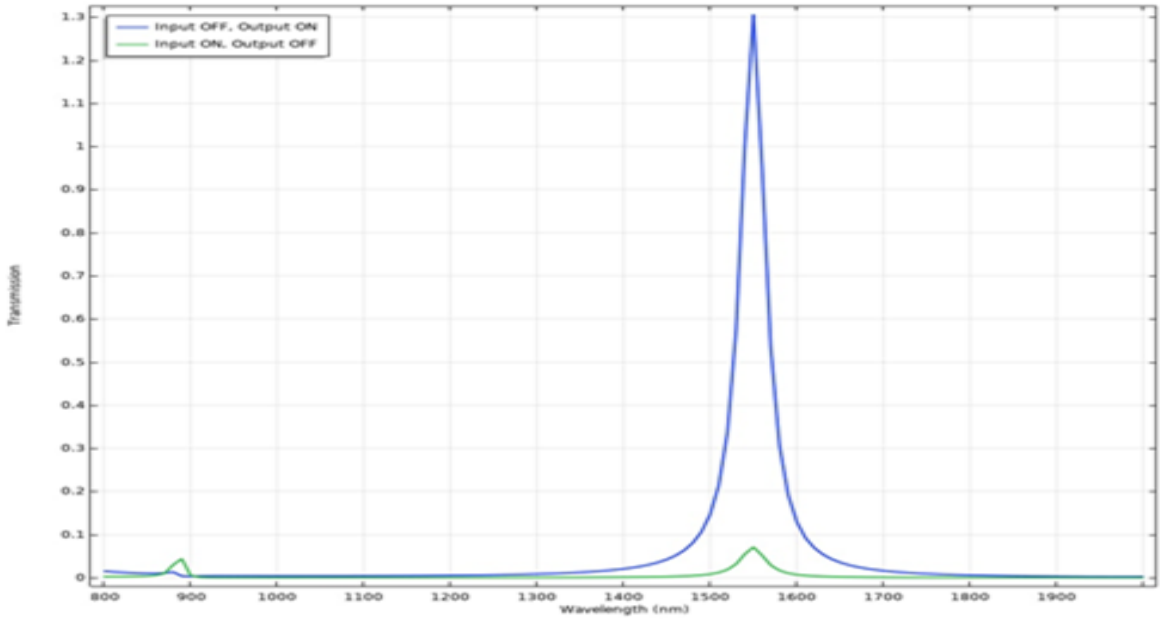


Figure. 3 Transmission curve Vs. wavelength range for NOT gate

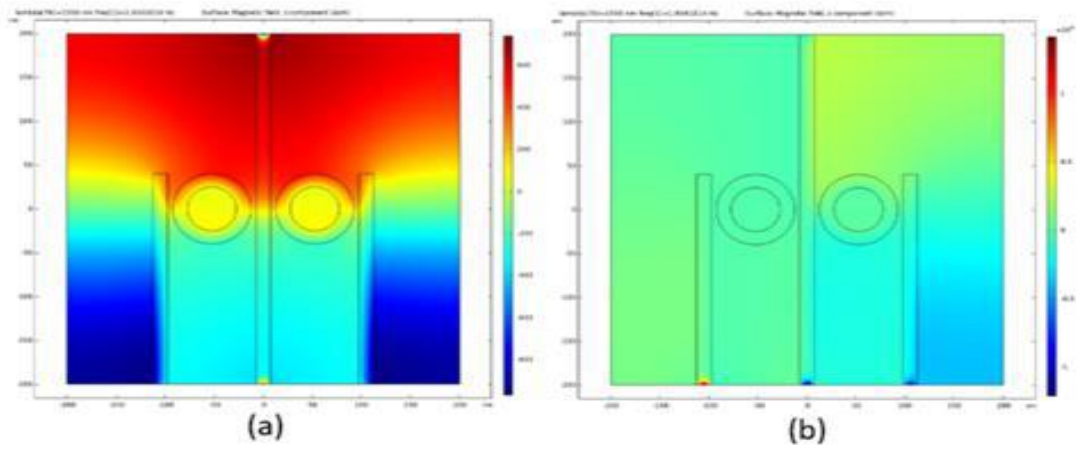


Figure. 4 Distribution of magnetic field (a) first case and (b) second case for NOT logic gate

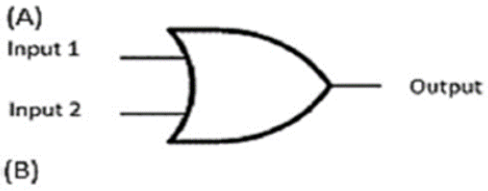
Table 3. NOT gate transmission

In (Phase)	Control 1(Phase)	Control 2(Phase)	T	T_{th}	Output Port
OFF(0°)	ON(0°)	ON(0°)	1.306	0.5	ON
ON(0°)	ON(180°)	ON(45°)	0.071	0.5	OFF

According to CR Equation, the plasmonic NOT gate's CR is 12.64 dB, which is considered high value, and its performance is very good and efficient. While the MD value is 94.56% according to MD Equation, this is considered a very high value, and the suggested structure dimensions are optimum and excellent. IL value is -1.159 dB according IL equation.

OR Logic gate

The current proposed structure implements an OR gate by making executors 1 and 2 input executors, executor 3 a control executor, and making executor 4 an output executor, as illustrated in Fig. 1. OR gate is a gate which produces logic 1 in the second, third, and fourth states of its truth table but logic 0 in the first. Fig. 5 (a) and (b) depict OR gate's symbol circuit and truth table, respectively.



(B)

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Figure. 5 (A) OR gate's symbol circuit (B) OR gate truth table

This gate's function is accomplished through constructive interferences between signals of light dispersed in the input and control executors in second, third and fourth cases so the output executor will be ON. In the first case the input executors are OFF and only control executor is ON so output executor is OFF. Fig. 6 depicts the transmission versus wavelength range curve for the plasmonic OR gate. Fig. 7 depicts the distribution of magnetic field of all cases. Table 4 describes the validation of the proposed plasmonic OR gate.

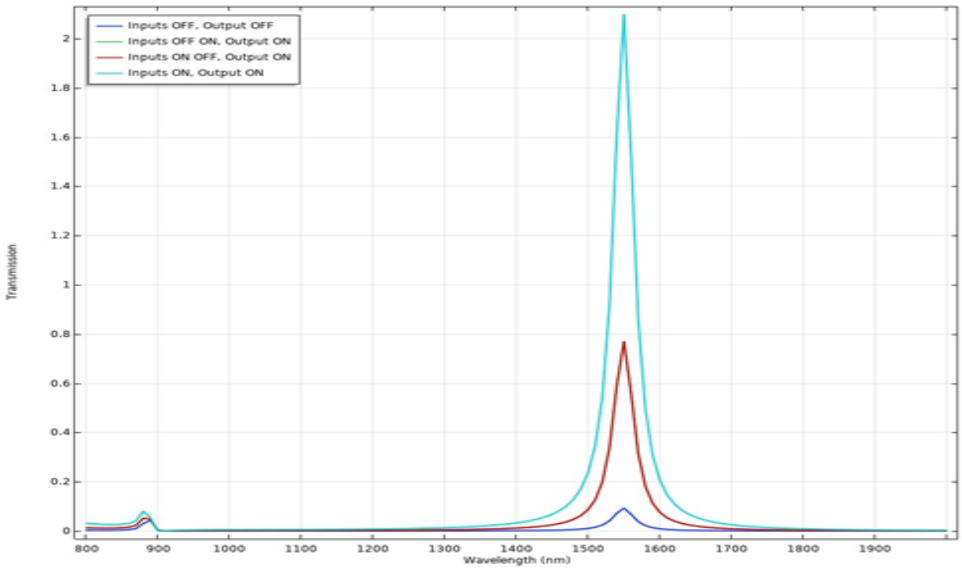


Figure. 6 Transmission curve Vs. wavelength range for OR logic gate

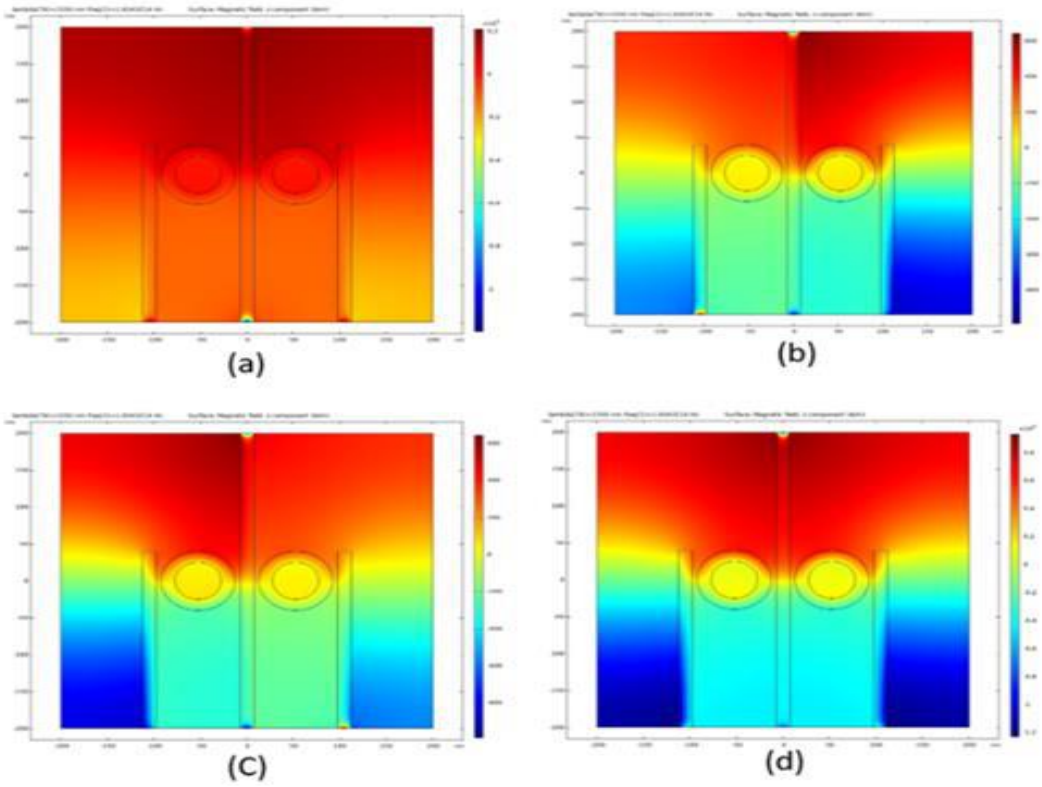


Figure. 7 (a), (b), (c), (d) magnetic field distribution for all cases for OR logic gate, respectivly

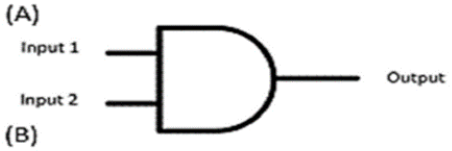
Table 4. OR gate transmission

In 1(Phase)	IN 2(Phase)	Control (Phase)	T	T_{th}	Output Port
OFF(0°)	OFF(0°)	ON(0°)	0.0937	0.5	OFF
OFF(0°)	ON(0°)	ON(0°)	0.77	0.5	ON
ON(0°)	OFF(0°)	ON(0°)	0.77	0.5	ON
ON(0°)	ON(0°)	ON(0°)	2.1	0.5	ON

According to CR Equation, the plasmonic OR gate's CR is 9.147 dB, which is considered medium value, and its performance is good and efficient. While the MD value is 95.53% according to MD Equation, this is considered a very high value, and the dimensions of suggested structure are optimum and excellent. IL value is 1.135 dB according IL equation.

AND logic gate

The current proposed structure implements an AND gate by making executors 1 and 2 input executors, executor 4 a control executor, and executor 3 an output executor, as illustrated in Fig. 1. AND gate is a gate which produces logic 0 in the first, second, and third states of its truth table but logic 1 in the fourth. Fig. 8 (a) and (b) depict the AND gate's symbol circuit and truth table, respectively.



Input 1	Input 2	output
0	0	0
0	1	0
1	0	0
1	1	1

Figure. 8 (A) Symbol circuit of AND gate (B) AND gate truth table

In the first state, the input executors are OFF and only control executor is ON so output executor will be OFF. In the second and third states, when one of the input executors is ON with phase 180°, destructive interference occurs because of phase varying and the propagation's direction of the control and input signals, and the output will be OFF in the output executor. In the fourth state, constructive interference occurs because all control and input executors are ON and in similar phase so the output executor is ON state. Fig. 9 depicts the transmission versus wavelength range curve for the plasmonic

AND gate. Fig. 10 depicts the distribution of magnetic field of all cases. Table 5 describes the validation of proposed plasmonic AND gate.

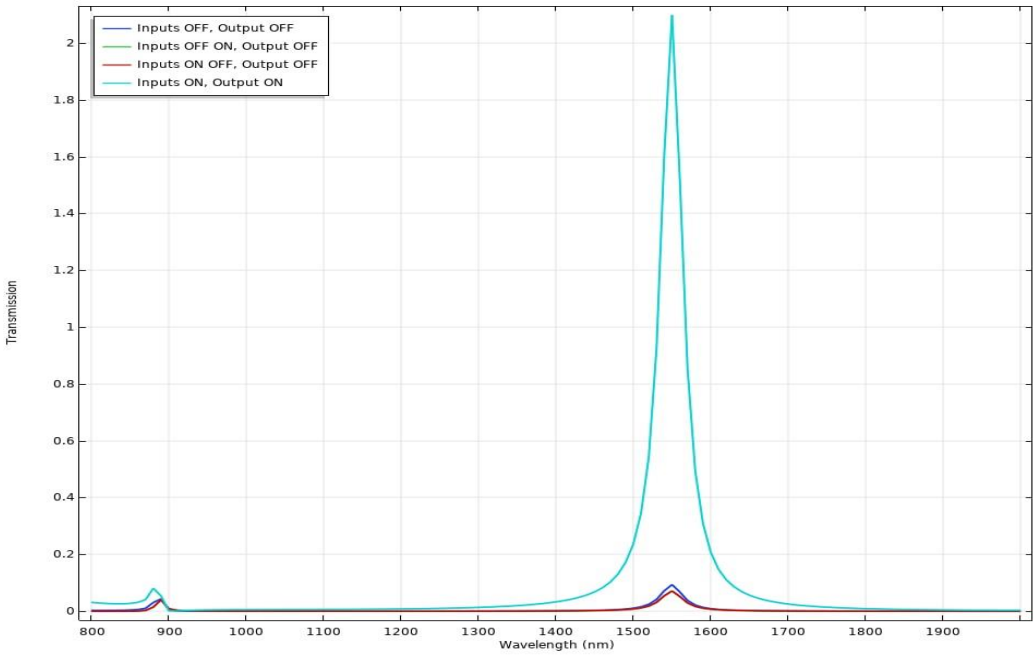


Figure. 9 The transmission curve Vs. the wavelength range for AND logic gate

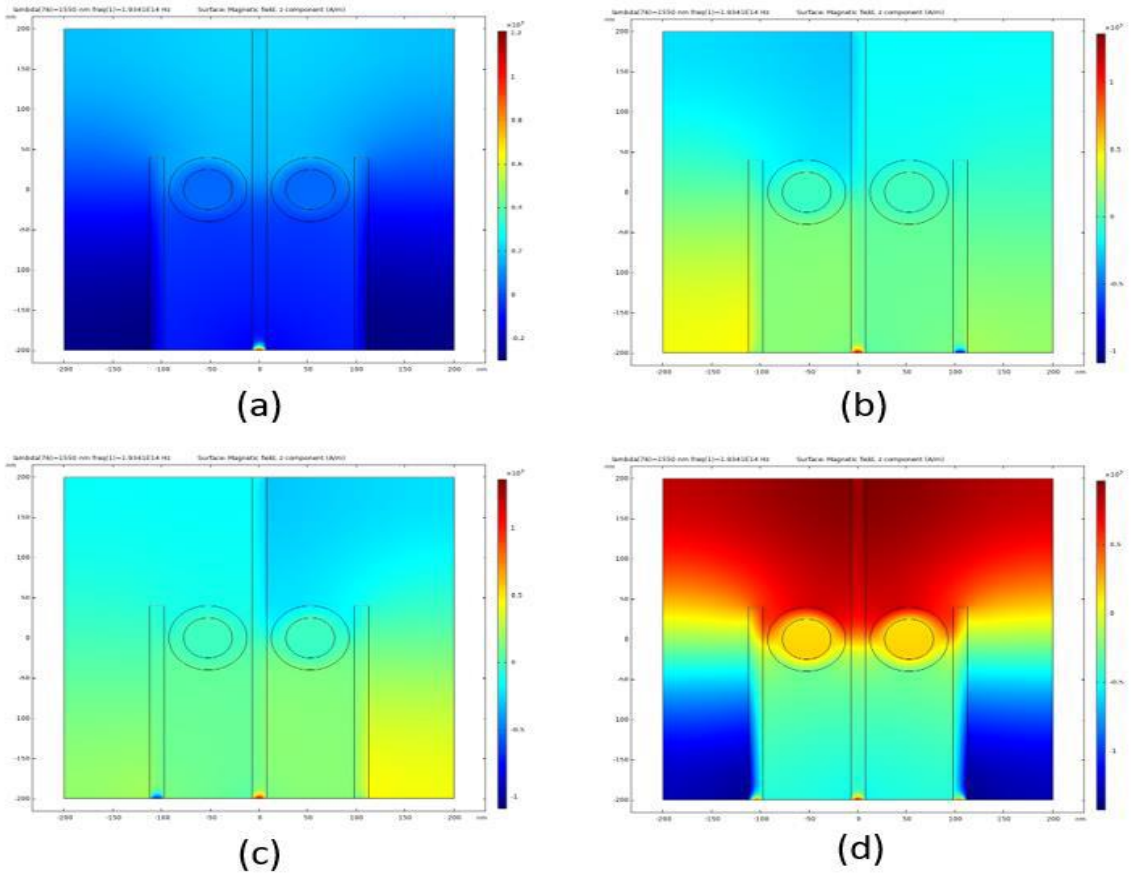


Figure. 10 (a), (b), (c), (d) Distribution of magnetic field for all cases for AND logic gate, respectively

9

Table 5. AND gate transmission

In 1(Phase)	IN 2(Phase)	Control (Phase)	T	T_{th}	Output Port
OFF(0°)	OFF(0°)	ON(180°)	0.093	0.5	OFF
OFF(0°)	ON(0°)	ON(180°)	0.071	0.5	OFF
ON(0°)	OFF(0°)	ON(180°)	0.071	0.5	OFF
ON(180°)	ON(180°)	ON(180°)	2.1	0.5	ON

According to CR Equation, the plasmonic AND gate's CR is 13.5 dB, which is considered high value, and its performance is very good and efficient. While the MD value is 96.6 according to MD Equation, this is considered a very high value, and the dimensions of the suggested structure are optimum and excellent. IL value is -3.222 dB according IL equation.

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Comparison of the suggested work and prior work

Table 6. compares the plasmonic gates that suggested to the early studies.

Criteria	[25]	[26]	[27]	[28]	[29]	This paper
Proposed fundamentals logic gates	OR, AND, NOT.	OR, NOT,	OR, AND, NOT.	OR, AND, NOT.	AND, OR, NOT.	NOT, OR, AND.
Plasmonic waveguide	IMI	MIM	MIM	MIM	MIM	IMI
Number of models that realize the logic gates	One structure	Three structure	One structure	One structure	One structure	One structure
Size(s)	200nm*400nm	2um*1.2um	1.5um*1um	600nm*600nm	1269nm*1269nm	400nm*400nm
Operating wavelength	1550nm	1300nm 1620nm	618nm 1191nm	1550nm	1200nm,885nm 800nm,1400nm	1550nm
Maximum transmission %	152	35	143	190	95	210
Performance measured	T, CR	T	T, CR, Gap-Threshold ratio (GTR)	T, CR	T	T, CR, MD,IL
Threshold of transmission	30%	10%	20%	35%	AND 28% OR 20% N0T 20%	0.5

Conclusion

This paper proposed, designed, and demonstrated plasmonic logic gates (NOT, OR, AND) in a new configuration based on nano-rings IMI plasmonic waveguides. The task of the suggested plasmonic logic gates has come to be realized through destructive and constructive interferences between both the control signal and the input signal(s). At the output, the Transmission threshold between states 1 and 0 is 0.5. The suggested plasmonic gates can be realized by making proper executor assignment choices in the proposed structures, as well as the proper phase angle selection, which results in destructive and constructive interferences. Four parameters are applied to evaluate the proposed structure's

performance: transmission, contrast ratio, modulation depth and insertion loss. Structure shape, structure size, structure parameters, materials used, selected materials refractive index, position of the executors in the structure, and phase can all be used to control the transmission at the output port. SPP is generated at 1550 nm. depending on its size, shape, parameters, and structure materials. This device had the following characteristics: transmission exceeds 100% in one state of all three gates, with medium and high contrast ratio values, very high modulation depth values, a small area, and an operating wavelength of 1550 nm. In the future, this technology will provide accessibility to nanophotonic integrated circuits and is viewed as a basic building element for all-optical computers.

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11

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