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All-Optical Universal Logic Gates at Nano-scale Dimensions

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Abstract

Though photonics displays an attractive solution to the speed limit of electronics, decreasing the size of photonic devices is one of the major problems with implementing photonic integrated circuits that are regarded as the challenges to produce all-optical computers. Plasmonic can solve these problems, it is a potential solution to fill the gaps in the electronics (large bandwidth and ultra-high-speed) and photonics (diffraction limit due to miniaturization size). In this paper, Nano-rings Insulator-Metal-Insulator (IMI) plasmonic waveguides have been used to propose, design, simulate, and perform all-optical universal logic gates (NOR and NAND gates). By using the Finite Element Method (FEM), the structure of the proposed plasmonic universal logic gates are designed and numerically simulated by two dimensions (2-D) structure. Silver and Glass materials were chosen to construct the proposed structure. The function of the proposed plasmonic NOR and NAND logic gates was achieved by the destructive and constructive interferences principle. The performance of the proposed device is measured by three criteria; transmission, extension ratio, and modulation depth. Numerical simulations show that a transmission threshold (0.3) that allows achieving the proposed plasmonic universal logic gates in one structure at 1550 nm operating wavelength. The properties of this device were as follows: The transmission exceeds 100% in one state of NAND gate, medium values of Extension Ratio, very high MD values, and very small footprint. In the future, this device will be the access to the nanophotonic integrated circuits and it has regarded fundamental building block for all-optical computers.

Introduction

In the rapidly improving photoelectric technology process, using optical waveguides to transmit and receive a signal is one of the best ways to increase the internet bandwidth (capacity) and speed. The confinement process of relatively high optical intensity in a small guiding space (ranging about a few tens of nanometers) is achieved by waveguide structures. Much of the recently published scientific research has paved the way for the use of this technique (optical waveguides) in many applications, especially in optical communications systems and in photonic integrated circuits. Utilizing optical devices in these two applications has many advantages like higher communication bandwidth and higher transmission speed in optical communications systems and nanometer-scale size, high capacity, ultrahigh-speed information processing, security to electromagnetic interference, low power consumption, and overcoming the diffraction limit in photonic integrated circuits. Sub-wavelength devices mean plasmonic devices. The study of plasmonics is a brunch of Optoelectronics/Nanophonics Engineering. In recent years, all-optical logic devices based on plasmonic technology have been the topic of comprehensive research. Plasmonic technology is a new technique that overcomes the obstacles in electronic devices performance limitations, which suffer from high heat generation and ingrained delay, as well as to overcome the diffraction limit that is the major obstacle in photonics devices. Thus, using plasmonic devices enabled manipulating light on a sub-wavelength scale; that is the reason why named the plasmonic is a subwavelength [1]. The process of interaction of electromagnetic waves with the free electrons in metals is called Surface Plasmon Polaritons (SPPs). SPPs are propagating on the metal-dielectric interface [2-3]. It is a collective wave where billions of electrons oscillate in synchronization at optical frequencies. Plasmons can travel along nanoscale wires. Recently, many structures that perform plasmonic technology proposed universal logic gates [4-8]. Each structure has a different way to realize the function of the universal gates, different geometries, different materials of the structure, different numbers of universal logic gates, different types of universal logic gates, different values of resonance wavelength, and different values of transmission.

This paper offers the smallest structure from other structures that perform plasmonic universal logic gates and in the same structure. The materials, structure parameters, resonance wavelength, and transmission threshold in both structures are the same. The structure is constructed with a Nano-rings resonator and Insulator-Metal-Insulator (IMI) plasmonic Nano-waveguides. The plasmonic universal logic gates proposed, designed, simulated, and realized are NOR and NAND. The simulation results obtained by COMSOL Multiphysics package software (version 5.3a) are based on the Finite Element Method (FEM). In the future, this device will be the access to the nanophotonic integrated circuits, and it has regarded fundamental building block for all-optical computers.

Theoretical Concepts

Plasmonic waveguides are used to guide the SPPs signal between dielectric-metal interfaces. Two types of waveguides are mostly used in plasmonic structures recently: insulator-metal-insulator (IMI) plasmonic waveguides and metal-insulator-metal (MIM) plasmonic waveguides. Because IMI waveguides have more propagation length, less propagation loss, and are easier in fabrication [9]. Therefore, we chose IMI plasmonic waveguides rather than MIM plasmonic waveguides due to their benefits.

Our suggested design consists of two nano-rings resonators and three straight stripes to construct, which is based on an insulator metal-insulator (IMI) as shown in Figure 1 with parameters shown in Table 1. The proposed design is made of

two materials, the first is silver, which is a metal, the straight stripes and the nano-rings resonator are made of it and the second material is Glass with a refractive index equal to 1.52 that forms the remainder of this structure. The Silver permittivity is characterized by Johnson and Christy data [10].

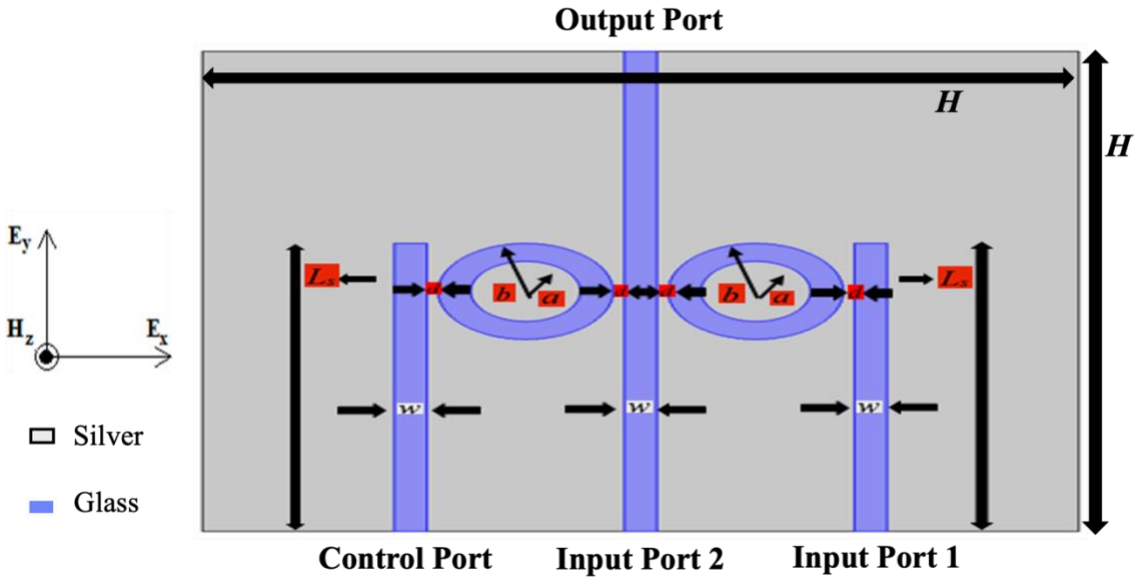


Figure 1 Plasmonic universal logic gates structure

Table 1. Structure parameters of the proposed design

Parameter	Description	Value
d	Distance between stripes and nano-rings	5 nm
w	Stripes width	15 nm
a	The smaller radius of nano-ring	25 nm
b	The bigger radius of nano-ring	40 nm
L_s	Length of the middle stipe	240 nm
H	Width and Length of the structure	400 nm

The operating wavelength is 1550 nm was chosen because it is the optimum wavelength in optical telecommunication systems. The type of interference when the two inputs and the control signal have the same phase is constructive interference. Otherwise, if the phase of the light wave of the inputs and control signal are different, destructive interference will happen. We conclude the phase difference causes a destructive interference between the waves [11].

Two-dimensional (2-D) structure in COMSOL Multiphysics software (version 5.3a) based on the FEM method is used to solve Maxwell equations. A plane wave with Transverse Magnetic (TM)-polarized that has Ex, Ey, and Hz electromagnetic field components are exposed to the proposed structure.

Four ports for the proposed structure, these ports as follows: two input ports, an output port, and a control port. According to the optimum results for the plasmonic universal logic gates, these ports are assigned. SPPs are excited when the input port(s) and control port are launched by a plane wave with TM-polarized. The performance of the proposed device is measured by three criteria: the first is the borderline between Logic 0 and Logic 1 at the output that is called transmission, the transmission is defined by Equation 1 [12-13]. Logic 0 and logic 1 are separated by 0.3, which is the transmission threshold value. The second is the extension or contrast ratio. This criterion is described by Equation 2 [12]. The third is modulation depth (MD), MD is defined by Equation 3 [14-15].

$$T = \textit{Output optical Power / Input Optical Power} \quad (1)$$

Where T is the transmission.

$$\textit{Extension Ratio (dB)} = 10 \log \left(\frac{P_{out}|ON}{P_{out}|OFF}\right) \quad (2)$$

Where: $P_{out}|ON$ is the minimum output power in ON state and $P_{out}|OFF$ is the maximum output power in the OFF state.

$$\textit{Modulation Depth (MD)} = \left(\frac{T_{ON}|Max - T_{OFF}|Min}{T_{ON}|Max}\right) \times 100\% \quad (3)$$

Where: $T_{ON}|Max$ is the maximum transmission in ON state and $T_{OFF}|Min$ is the minimum transmission in the OFF state.

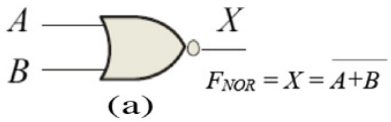
Simulation Results and Discussion

The performance of all-optical NOR and NAND logic gates by discussing the simulation results will be presented in this section. The proposed structure is exposed by a light wave with (800 nm - 2000 nm) wavelength range. This band is used because it is the most useful band in optical communication. The illumination of light is launched to the control port and the input port(s) (ON state). The function of each proposed plasmonic gate is achieved by two factors:

The right choice for assigning structure ports. The right choice of the phase angle, which makes the destructive and constructive interferences between light in input ports and the light in the control port.

A. All-Optical NOR Logic Gate

NOR gate is a gate that produces logic 0 at the second, the third, and the fourth states in its truth table, but at the first state produces logic 1. Figure 2(a) and 2(b) show the symbol and truth table of the NOR gate, respectively.



Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

(b)

Figure 2 (a) NOR logic gate symbol, and (b) NOR logic gate truth table

The proposed structure which performs a plasmonic NOR logic gate was shown in Figure 1. NOR gate can be achieved by destructive interference in the second, third, and fourth states. In the first state, the input ports are OFF, but a light to the control port is launched wavelength and phase always equal to 1550 nm and 180°, respectively. The output port is ON in this state, the transmission is 0.3265 that is above the threshold value. In the second state, the phase of the input light to input port 2 is 45°. The output port is OFF; the transmission in this state is 0.0723 that is below the threshold value. In the third state, the phase of the input light to input port 1 is 45°. The output port is OFF, the transmission in this state is 0.0025 that is below the threshold value. In the fourth state, the phase of the input light to the input ports (1 and 2) is 45° and 0°, respectively. The output port is OFF in this, the transmission is 0.071 that is below the threshold value. Due to the phase difference, destructive interference occurred in the last three states between the input signal(s) and the control signal. The curve of transmission with wavelength range for the plasmonic NOR logic gate is shown in Figure 3. The validation of the proposed plasmonic NOR logic gate is explained in Table 2.

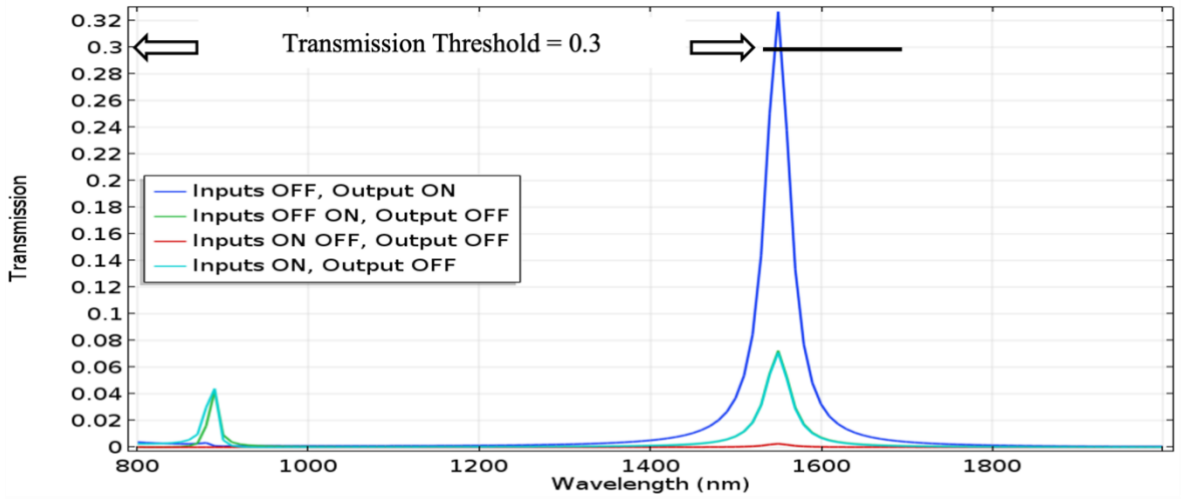


Figure 3 The transmission curve Vs. the wavelength range for NOR logic gate

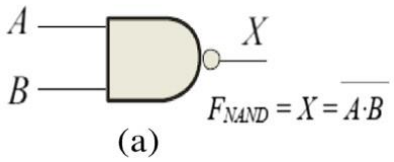
Table 2. Validation of the proposed plasmonic NOR logic gate

State 1	State 2	In 1 (Phase)	In 2 (Phase)	Control (Phase)	*T*	$T_{thresh.}$	Output	Output Port
0	0	OFF(0°)	OFF(0°)	ON(180°)	0.3265	0.3	1	ON
0	1	OFF(0°)	ON(45°)	ON(180°)	0.0723		0	OFF
1	0	ON(45°)	OFF(0°)	ON(180°)	0.0025		0	OFF
1	1	ON(45°)	ON(0°)	ON(180°)	0.071		0	OFF

According to Equation 2, the value of extension ratio of the plasmonic NOR gate is 6.55 dB that is regarded as medium value and the performance of this gate is moderate according to [12]. While the value of MD is 99.2% (According to Equation 3) that is regarded very high value and the dimensions of the proposed structure is excellent and optimum.

B. All-Optical NAND Logic Gate

NAND gate is a gate that produces logic 1 at the first, the second, and the third states in its truth table, but at the fourth state produce logic 0. Figure 4(a) and 4 (b) show the symbol and truth table of the NAND gate, respectively.



(a)

Inputs		Output
A	*B*	*X*
0	0	1
0	1	1
1	0	1
1	1	0

(b)

Figure 4 (a) NAND logic gate symbol, and (b) NAND logic gate truth table

The proposed structure, which performs a plasmonic NAND logic gate, is shown in Figure 1. NAND gate can be achieved by constructive interference in the second and third states and by destructive interference in the fourth state. The input ports are OFF in the first state, but a light to the control port is launched wavelength and phase always equal to 1550 nm and 0°, respectively. The output port is ON in this state, the transmission is 0.3265 that is above the threshold value. In the second state, the phase of the input light to input port 2 is 0°. The output port is ON, the transmission in this state is 0.77 that is above the threshold value. In the third state, the phase of the input light to input port 1 is 0°. The output port is ON in this

state, the transmission is 1.306 that is above the threshold value. In the fourth state, the phase of the input light to the input ports (1 and 2) is 180° and 90°, respectively. The output port is OFF in this state, the transmission 0.0425 that is below the threshold value. The curve of transmission with wavelength range for plasmonic NAND logic gate is shown in Figure 5. The validation of the proposed plasmonic NAND logic gate is explained in Table 3.

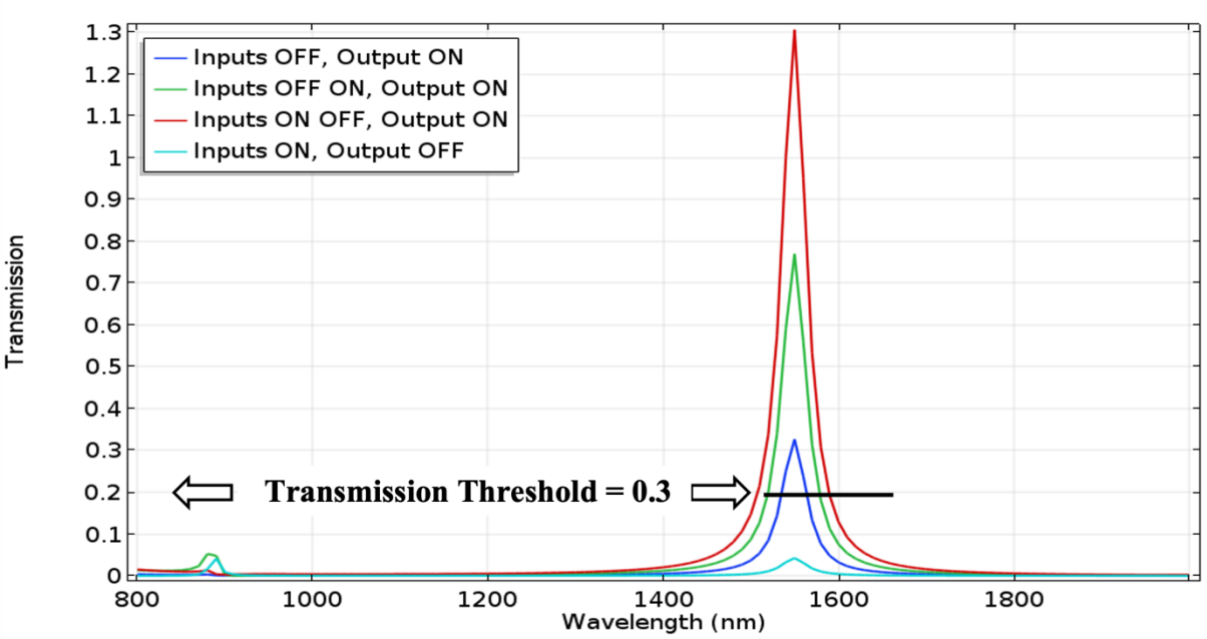


Figure 5 The transmission curve Vs. wavelength range for NAND logic gate

Table 3. Validation of the proposed plasmonic NAND logic gate

State 1	State 2	In 1 (Phase)	In 2 (Phase)	Control (Phase)	T	$T_{thresh.}$	Output	Output Port
0	0	OFF(0°)	OFF(0°)	ON(0°)	0.3265	0.3	1	ON
0	1	OFF(0°)	ON(0°)	ON(0°)	0.77		1	ON
1	0	ON(0°)	OFF(0°)	ON(0°)	1.306		1	ON
1	1	ON(180°)	ON(90°)	ON(0°)	0.0425		0	OFF

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According to Equation 2, the value of extension ratio of the plasmonic NAND gate is 8.85 dB that is regarded as a medium value and the performance of this gate is Good and efficient according to [12]. While the value of MD is 96.75% (According to Equation 3) that is regarded very high value and the dimensions of the proposed structure are excellent and optimum.

Comparison with Previous Works

Plasmonic universal logic gates in this work are compared with the other previous papers as shown in Table 4.

Table 4. Comparison between this paper and the other previous papers.

Criteria / Paper	This Paper	Reference [4]	Reference [5]	Reference [6]	Reference [7]	Reference [8]
Topology	IMI Waveguide	Plasmonics Kerr effect based Mach-Zehnder interferometer (MZI)	MIM Waveguide	MIM Waveguide	MIM Waveguide	MIM Waveguide
Dielectric / Metal Used	Glass / Silver	Non-Linear Kerr Material	Air / Silver	Air / Silver	Non-Linear Kerr Material	Non-Linear Kerr Material
Permittivity Metal Description	Johnson Data	--------	Drude Model	--------	--------	Drude Lorentze model
Number of Proposed Universal Logic Gates	Two Gates	Two Gates	One Gate	One Gate	One Gate	One Gate
Type of Universal Gates	NOR and NAND	NOR and NAND	NOR	NAND	NAND	NAND
Size	400 nm × 400 nm	45 um × 8 um	More than 3 um × 2 um	40 um × 7.5 um	40 um × 7.5 um	36 um × 8 um
Performance Measured	Transmission, Extension Ratio, and MD	Extension Ratio and Insertion Loss	Transmission and Extension Ratio	Insertion Loss and Extension Ratio	Extension Ratio and Insertion Loss	Extension Ratio and Insertion Loss
Maximum Transmission %	130% at NAND Gate	--------	80.07 at NOR Gate	--------	--------	--------
Amplifying of Transmission	Exists in NAND Gate	--------	Does Not Exist	--------	--------	--------
Complexity in Fabrication	Less complexity	More Complexity	More Complicated	More Complicated	More Complexity	More Complexity

Conclusion

In this paper, plasmonic universal logic gates in a new configuration, which is based on nano-rings IMI plasmonic waveguides, were proposed, designed, and demonstrated. The borderline between state 1 and state 0 at the output is 0.3. By destructive and constructive interferences, which happen between the control signal and input signal(s), the function of the proposed plasmonic universal logic gates is realized. The proposed plasmonic universal logic gates can be achieved by the right choice for assigning the ports in the proposed structures (which is an input port(s), which is a control port, and which is an output port), and the right choice of phase angle which make the destructive and constructive interferences. The performance of the proposed structure is measured by three parameters; Transmission, Extension Ratio, and Modulation Depth (MD). The minimization or maximization of the transmission at the output port can be controlled by; structure shape, structure size, structure parameters, materials used in the structure, refractive index of the selected materials, the position of the ports in the structure, and its phase. In accordance with the size, shape, parameters, and materials of structure, the SPP is excited at a 1550 nm wavelength. The properties of this device were as follows: The transmission exceeds 100% in one state of NAND gate, medium values of Extension Ratio, very high MD values, very small area, and operating wavelength is 1550 nm. In the future, this device will be the access to the nanophotonic integrated circuits and it has regarded fundamental building block for all-optical computers.

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