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Nano-scale Investigation for Optical XOR and XNOR Logic Gates at 1.55 μm

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Abstract

In this article, nano-rings Insulator-Metal-Insulator (IMI) plasmonic waveguides are used to propose, simulate, design, and construct all-optical (XOR and XNOR) logic gates. The Finite Element Method (FEM) has been used to develop and numerically simulate the proposed two-dimensional (2-D) structure of plasmonic gates. Four metrics are used to assess the performance of the proposed device: insertion loss, modulation depth (MD), transmission, and extension ratio (ER). Glass and silver were used to build the suggested building. Destructive and constructive interferences were used to create the functioning of the proposed plasmonic gates. According to numerical simulations, the proposed plasmonic gates with a transmission threshold of (0.3) could be realized in a single structure operating at1.55 µm. The characteristics of this device were as follows: medium Extension Ratio values, high MD values, transmission above 200% in a single state of XNOR gate. This technology is also considered essential to all-optical computers and opening the door to future access to nanophotonic integrated circuits.

Introduction

Early in 1902, the Wood's anomaly a region of the light spectrum emitted by a metal grating was discovered. This finding marked the start of scientific research on plasmonics [1]. Subsequently, a physical explanation was

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proposed for the Lord Rayleigh phenomenon [2], describing an anomaly in the light spectrum that results from light diffracted within a wavelength where a surface-occurring inadvertently dispersed wave develops. Next, the semi-stationary polarized waves were expected to resonate throughout the metal's surface. Cohesion, which is the result of excited electrons in the metal and was later dubbed surface plasmons, is what causes this energy loss [3]. Electromagnetic waves restricted to metal-dielectric interfaces are known as surface plasmon polaritons (SPPs), and they are linked to the propagation of free electronic oscillations on metal surfaces [4-6], and are believed to hold the most promise for the development of nanophotonic devices [7-9]. Researchers' interest in optical systems based on SPPs has increased in recent times because to the growing demand for high-speed, high-bandwidth data transmission. SPPs devices surpass limitations of electrical devices, such as high heat generation and data transmission delay. (SPPs) help with sub-wavelength light processing as well as breaking beyond the diffraction limit in traditional optical systems. This characteristic prompted scientists to concentrate on the micro guiding structures that limit light that is sub-wavelength. Since plasmonic waveguides (SPPs) are the result of electromagnetic waves and free electrons of metals propagating across metal-insulating or insulating-metal interfaces, they have considerable promise for guiding patterns of sub-wavelength light [10,11]. Numerous Plasmonic waveguiding structures, such as resonators [12], modulators [13], switches [14], nanocavities [15], nanowires [16], Bragg reflectors [15], multi/demultiplexers [17], and logic gates [18-21] and so on, have been proposed. Each structure in the field of logic gates has a unique way of carrying out the function, a variety of geometries, a variety of materials, a variety of numbers and types of logic gates, a variety of resonance wavelength values, and a variety of transmission values. In this research, a structure that can simultaneously operate three plasmonic logic gates (XOR and XNOR) is proposed. The materials, resonance wavelength, transmission threshold, and structural parameters are all the same. Insulator-Metal-Insulator (IMI) plasmonic Nano-waveguides and a Nano-rings resonator are used in the construction of the structure. The simulation results obtained by COMSOL Multiphysics (version 5.4) are based on the Finite Element Method (FEM). This method has been viewed as a keystone for all-optical computers and will enable the fabrication of nanophotonic integrated circuits in the future. The format of this scientific article is as follows: All of the methodology's steps, materials, and mathematical models are covered in Section 2. The results are presented and discussed in Section 3. This work is compared to earlier ones in Section 4. Section 5 closes with final remarks conclusion.

Methodolog and Layout Structure

Plasmonic waveguides are used to direct the SPPs signal between dielectric-metal surfaces. In recent times, insulator-metal-insulator (IMI) and metal-insulator-metal (MIM) plasmonic waveguides have been extensively utilized in plasmonic structures. IMI waveguides are easier to build, offer a longer propagation length, and less propagation loss [18]. We selected IMI plasmonic waveguides over MIM plasmonic waveguides due to these

benefits. Two nano-ring resonators and three stripes make up the proposed architecture for executing Plasmonic gates (XOR and XNOR), as shown in Fig. 1. Glass serves as the dielectric material for the remainder of the framework, while silver is used for the stripes and the nano-ring resonator.

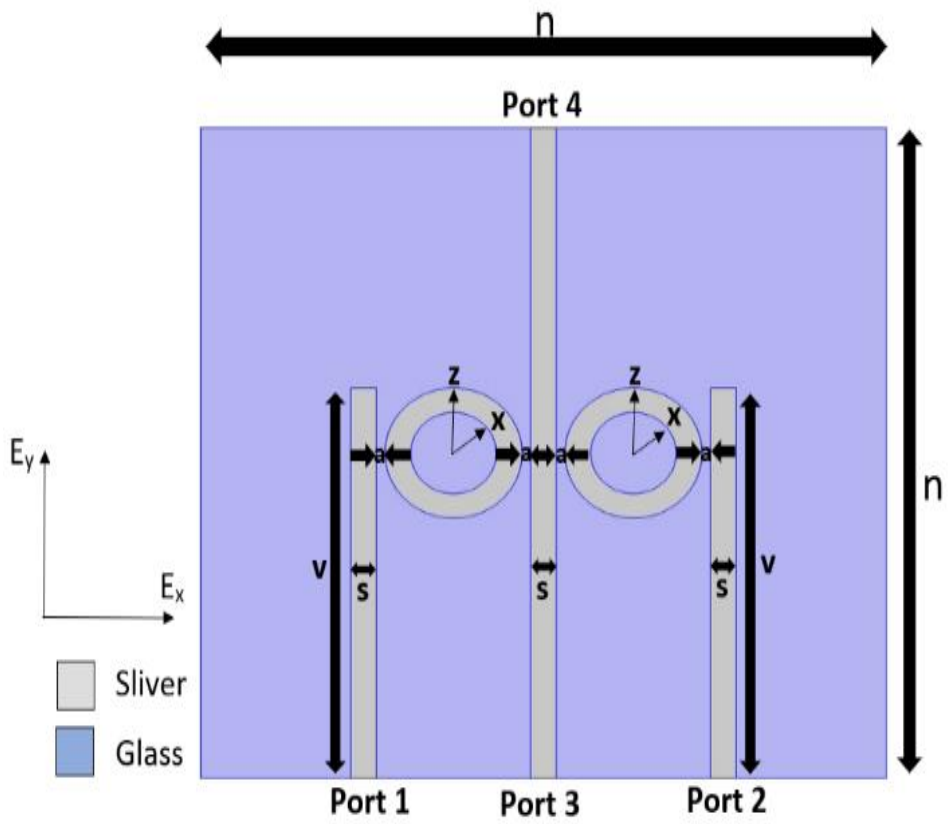


Figure. 1 Plasmonic gate structure

The dielectric refractive index for the Glass is 1.52 [20], and the silver permittivity is based on data from Johnson and Christy [22]. The properties of the proposed structure are displayed in Table 1.

Table 1. Structure specifications for the suggested design

Parameter	Description	Value (nm)
a	Distance between stripes and nano-rings	5
s	Stripes width	15
x	The smaller radius of nano-ring	25

z	The bigger radius of nano-ring	40
v	Length of the side stipe	240
n	Width and Length of the structure	400

Plasmonic logic gates have uniform dimensions, sizes, and construction materials. The operational wavelength of at1.55 μm was selected because it is the best wavelength for optical telecommunication networks. The size, form, materials, and structural elements of the suggested construction enable the resonance wavelength of 1550 nm. Using the FEM method, Maxwell equations were solved in the two-dimensional (2D) framework of the COMSOL Multiphysics program. The framework, which has four ports as shown in Fig. 1, is exposed to a plane wave with Transverse Magnetic (TM) components E_x, E_y, and H_z. Based on four criteria: transmission [19], contrast ratio (CR) [19], modulation depth (MD) [19], and insertion loss (IL) [23], the proposed all-optical logic gates are functional at at1.55 μm. The performance's equations are shown in Table 2.

Table 2. Performance's equations

Parameter	Equation
T	$\frac{Output\ optical\ Power}{Input\ Optical\ Power}$
ER (dB)	$10 \log \left(\frac{P_{out\|ON/min}}{P_{out\|OFF/max}}\right)$
MD (%)	$\left(\frac{T_{ON\|Max} - T_{OFF\|Min}}{T_{ON\|Max}}\right) \times 100\%$
IL (dB)	$-10 \log \left(\frac{P_{out\|ON/min}}{P_{in}}\right)$

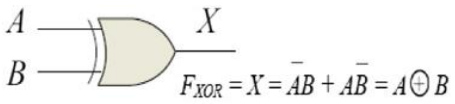
Whereas Pin denotes the input's optical power 1 uw that reached a single input port or control port, Pout denotes the output optical power. The main concept behind the proposed all-optical logic gates is the employment of both destructive and constructive interferences. The presence of two or more signals with the same phase results in constructive interference. On the other hand, the phase mismatch between the incident light signals on the structure causes destructive interference. This concept is applied in logic 1 and logic 0 to each gate's truth table.

Discussion of Simulation Results

The transmission is determined in both the OFF and ON states, and a transmission threshold value is established to determine whether the state is OFF or ON. A series of specifications led to the transmission threshold value of 0.3 being chosen in this design to implement the two logic gates [24].

1. XOR Logic Gate

The current proposed structure implements an XOR gate by making executors 1 and 2 input executors, executor 3 a control executor, and making executor 4 an output executor, as illustrated in Fig. 1. XOR gate is a gate which produces logic 1 in the second and third, while first and fourth states of its truth table is logic 0. Fig. 5 (a) and (b) depict XOR gate's symbol circuit and truth table, respectively.



(a)

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

(b)

Figure 5: (a) Symbol circuit of the XOR gate; (b) truth table of the XOR gate

The function of this gate is done through constructive interferences between light signals scattered in the input and control executors in the second and third such that the output executor is ON. In the first scenario, all input executors are turned off, and only the control executor is turned on, therefore the output executor is turned off. In the fourth stage, destructive interference occurs between the input and control ports, resulting in the output executor being turned off. The transmission versus wavelength range curve for the plasmonic XOR gate is shown in Fig. 6. Figure 7 displays the magnetic field distribution in all circumstances. The validation of the proposed plasmonic XOR gate is described in Table 4.

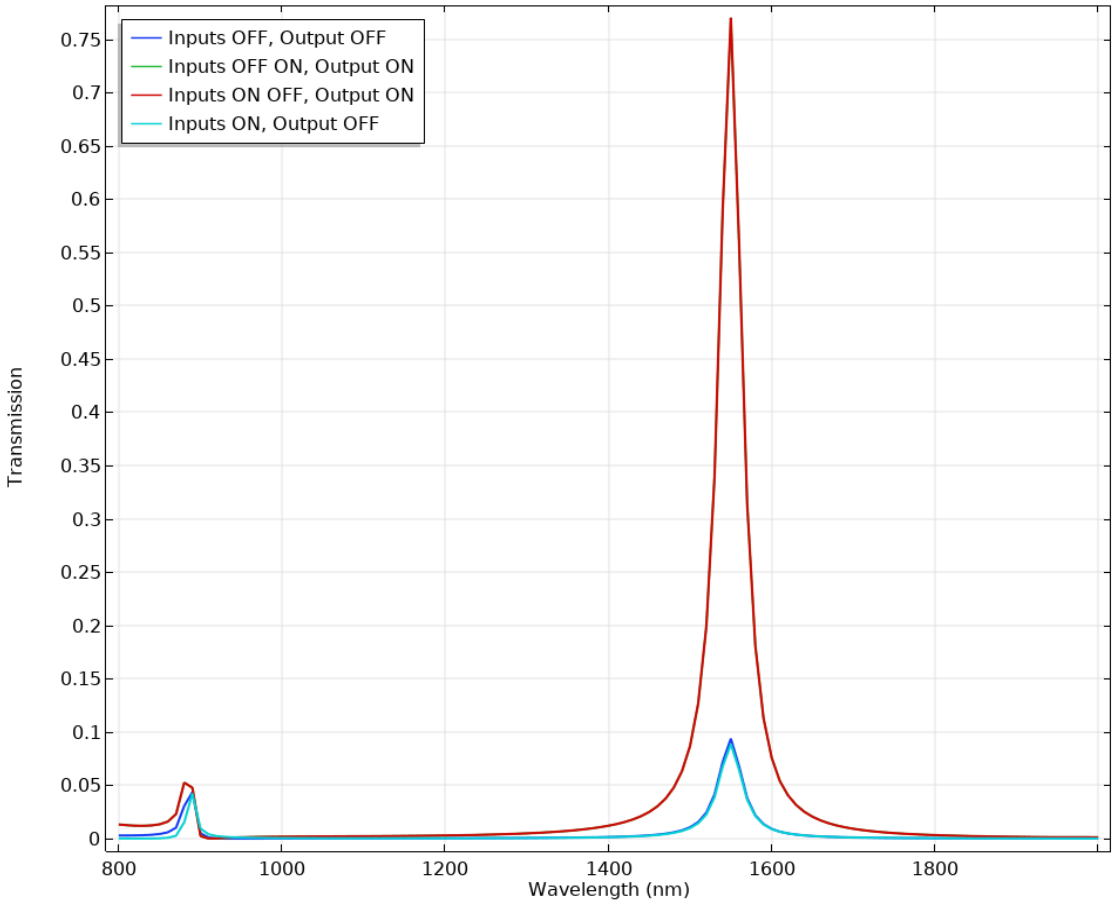
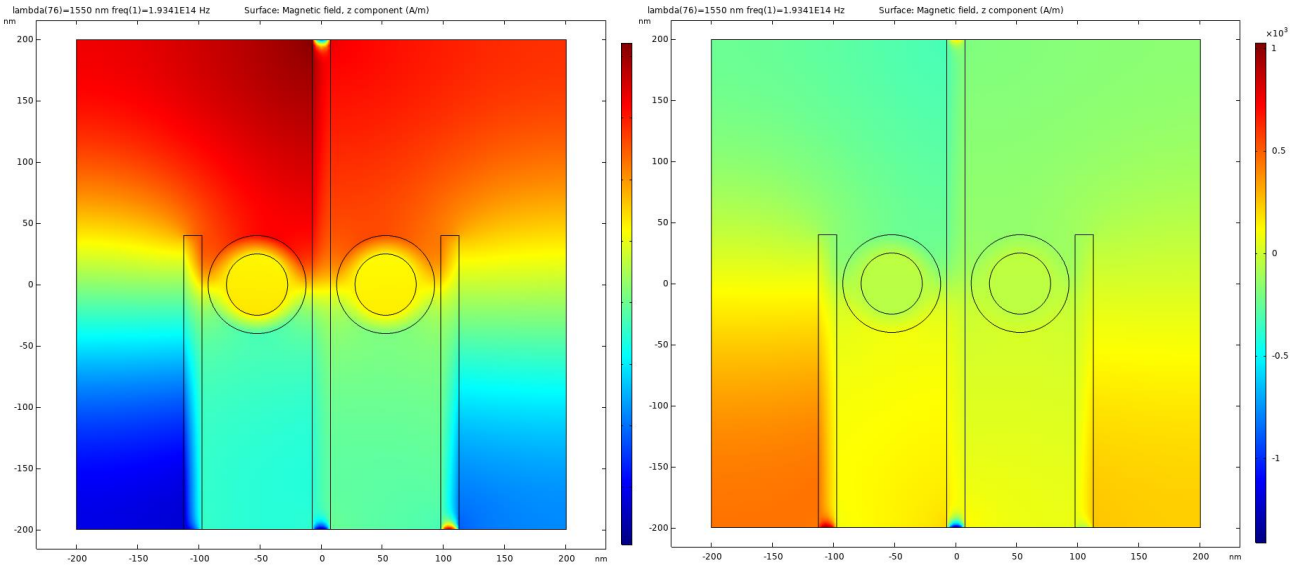


Figure 6: XOR logic gate transmission curve vs wavelength range



(a) (b)

Figure. 7 (a) and (b), magnetic field distribution for third (logic 1) and fourth (logic 0) cases for XOR logic gate, respectively

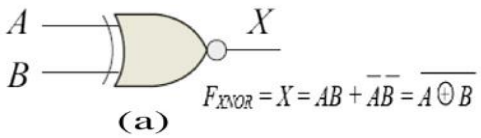
Table 4. XOR gate validation

In 1 (Phase)	In 2 (Phase)	Control (Phase)	T | T_{th}	Output Port
OFF(0°)	OFF(0°)	ON(0°)	0.0937 | **0.3**	OFF
OFF(0°)	ON(0°)	ON(0°)	0.77 | **0.3**	ON
ON(0°)	OFF(0°)	ON(0°)	0.77 | **0.3**	ON
ON(180°)	ON(90°)	ON(0°)	0.088 | **0.3**	OFF

The plasmonic XOR gate exhibits good and efficient performance, with an ER of 9.147 dB, which is deemed a medium value, as per the ER Equation. Although the MD Equation indicates that the MD value is 88.6%, this is still regarded as a high number, and the dimensions of the proposed construction are Excellent and Efficient. 1.135 dB is the IL value, based on the IL equation.

2. XNOR Logic Gate

The current proposed structure implements a XNOR gate by making executors 2 and 3 input executors, executor 1 a control executor, and executor 4 an output executor, as illustrated in Fig. 1. XOR gate is a gate which produces logic 0 in the second, and third states of its truth table but logic 1 in the first and fourth states. Fig. 8 (a) and (b) depict the XNOR gate's symbol circuit and truth table, respectively.



(a)

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	1

(b)

Figure 8 (a) XNOR gate symbol circuit; (b) XNOR gate truth table

In the initial state, the output executor will be ON based on the port's location and orientation as all input executors are OFF and only the control executor is ON. Phase variation between the control and input signals

causes destructive interference in the second and third states when one of the input executors (second and third states) is ON with phase 180°. As a result, the output of the output executor is turned off. Constructive interference happens in the fourth state when the output executor is in the ON state due to all control and input executors being ON and in a comparable phase. The transmission versus wavelength range curve of the plasmonic XNOR gate is shown in Fig. 9. The magnetic field distribution for second and fourth scenario is shown in Fig. 10. The validation of the suggested plasmonic XNOR gate is described in Table 5.

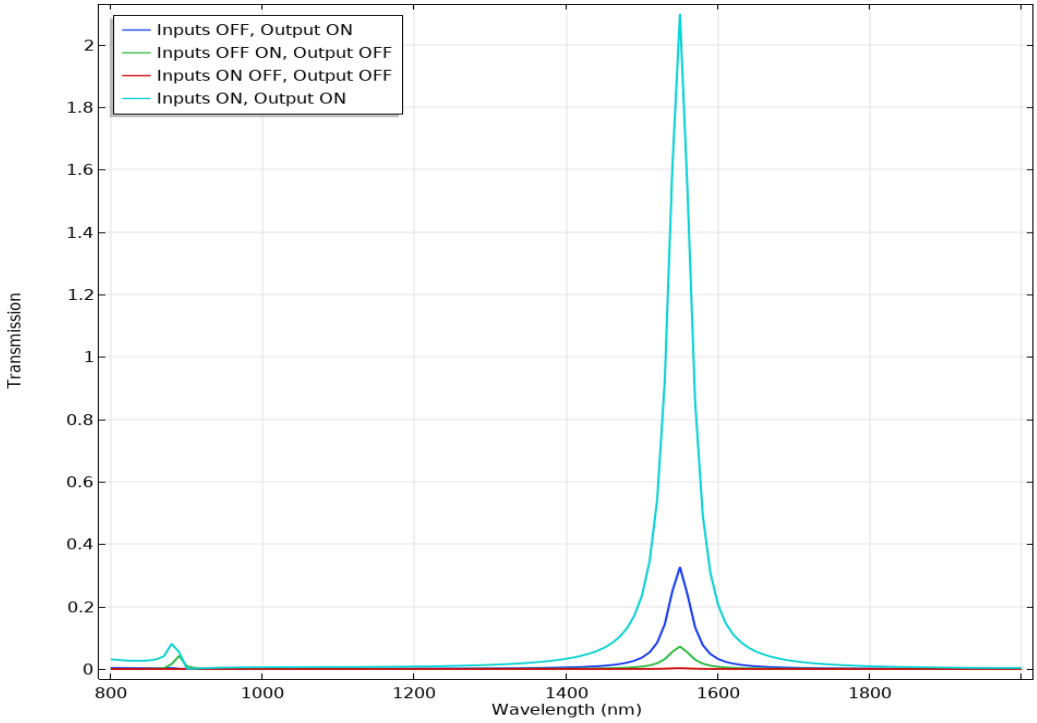
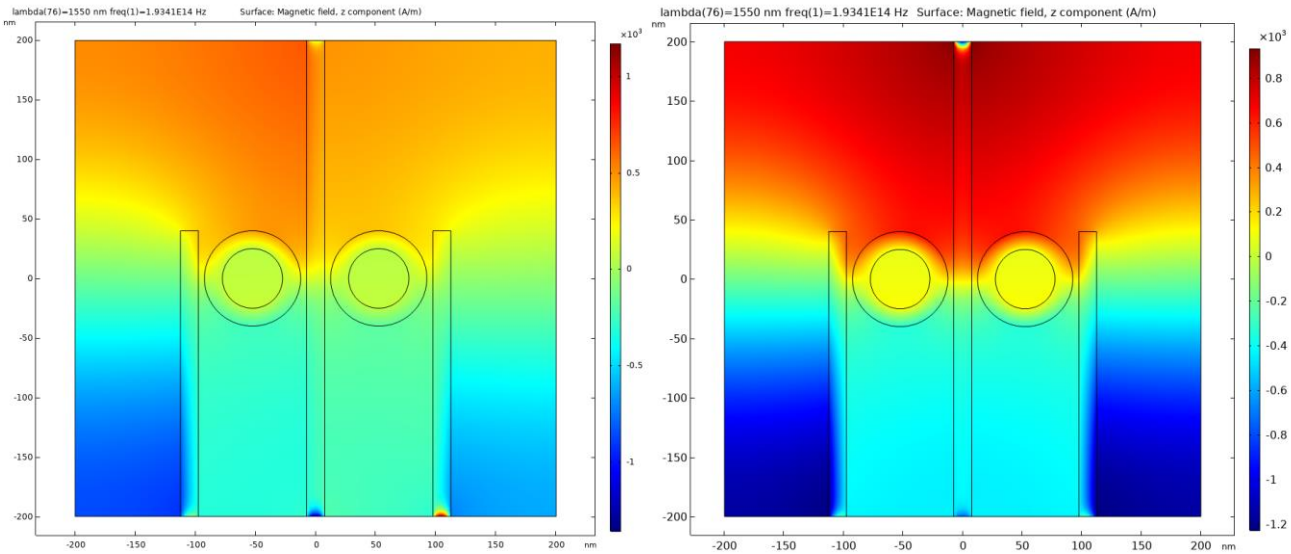


Figure 9: The XNOR logic gate's transmission curve vs wavelength range



(a) (b)

Figure. 10 (a) and (b) Distribution of magnetic field for second (logic 0) and fourth (logic 1) cases for XNOR logic gate, respectively

Table 5. XNOR gate validation

In 1 (Phase)	**In 2 (Phase)**	**Control (Phase)**	**T | T_{th}**	**Output Port**
OFF(0°)	OFF(0°)	ON(0°)	0.33 | **0.3**	ON
OFF(0°)	ON(180°)	ON(0°)	0.07 | **0.3**	OFF
ON(1800°)	OFF(0°)	ON(0°)	0.002 | **0.3**	OFF
ON(0°)	ON(0°)	ON(0°)	2.1 | **0.3**	ON

The plasmonic XNOR gate exhibits modest performance with an ER of 6.7 dB, which is considered the median value, as determined by the ER Equation. Although the MD value of 99.9 as determined by the MD Equation is regarded as exceptionally high, the dimensions of the proposed construction are optimal and excellent. The IL calculation indicates that the IL value is 4.8 dB.

4. Comparison between Previous Work and This Work

Table 6. Compares the proposed gates with modern previous papers.

Criteria	[25]	[26]	[27]	[28]	[29]	[30]	[31]	[32]	This paper
Topology	MIM	MIM	Hybrid IMI	MIM	Dielectric-loaded plasmonic	IMI	MIM	Insulator and Semiconductor	IMI
Proposed fundamentals logic gates	XOR, XNOR	XOR	XOR, XNOR	XOR	XNOR	XOR, XNOR	XOR	XOR, XNOR	XOR, XNOR
Operating wavelength(s)	None	1.55 um	1310 nm	600 nm and 1200 nm	780 nm	850 nm	870 nm	1.55 um	1.55 um
Structure Complexity	More	More	More	More	More	More	More	Less	Lesser

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Size	In micro meter range	In micro meter range	400 nm*400 nm	In micro meter range	In micro meter range	250 nm * 250 nm	1.5 um * 0.62 um	1.5 um * 1 um	400nm*400nm
Performance measured	T, CR	IL, CR	T, CR, MD, IL	Gap-Threshold Ratio (GTR), CR	CR	T, ER, MD, IL	T	T, CR	T, ER, MD, IL
Maximum transmission %	90	None	202.3	40	None	210	90	86	210

Conclusion

In this study, a new configuration of plasmonic logic gates (XOR and XNOR) based on nano-rings IMI plasmonic waveguides was proposed, constructed, and tested. The proposed plasmonic logic gates have achieved their goal by use of both constructive and destructive interferences between the input signal(s) and the control signal. The transmission threshold at the output, which separates states 1 and 0, is 0.3. By selecting the appropriate phase angle and executor assignment in the proposed structures, which leads to both constructive and destructive interferences, the recommended plasmonic gates can be implemented. The performance of the suggested structure is assessed using four parameters: transmission, contrast ratio, modulation depth, and insertion loss. The position of the executors within the structure, phase, materials utilized, refractive index of the chosen materials, size and dimensions of the structure, and other factors can all be used to influence the transmission at the output port. It generates SPP at 1550 nm. based on the components of its structure, characteristics, size, and shape. The characteristics of this device were as follows: it had a working wavelength of 1550 nm, a small area, medium and high contrast ratio values, high and very high modulation depth values, and transmission exceeding 200% in one state of the XNOR gate. This technology is seen as a fundamental component of all-optical computer and will make nanophotonic integrated circuits accessible in the future.

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